Terminal ASIC Structure for Satellite IoT transmission

Sooyeob Jung, Mi-Kyung Oh, Sangjae Lee, and Joon Gyu Ryu
Satellite Wide-Area Infra Research Section
Electronics and Telecommunications Research Institute
Daejeon, Rep. of Korea
Email: {jung2816, ohmik, leestrike, jgryurt}@etri.re.kr

***Abstract*—This paper presents the structure of terminal ASIC chip with low speed, low power, and small characteristics for satellite IoT transmission. The external connection with the sensor, flash external, and tuner will be made centering on the ASIC chip. Three transmission waveforms, such as the LoRa, I-LoRa, and LoRa-E, will be used to send the collected data to LEO satellite. As a result, the data collected from the sensor is transmitted to the ASIC chip through the sensor interface, and the ASIC chip modulates the collected data into an uplink signal and sends it to LEO satellite through the tuner.**

Keywords—ASIC, satellite IoT, LoRa, terminal

I. INTRODUCTION

The satellite Internet of Things (IoT) service enables the expansion of the IoT service to areas where terrestrial wireless signals cannot reach [1]. In particular, It is possible to provide global IoT services that can provide logistics monitoring services such as environmental monitoring and containers even in areas where it is difficult to build existing terrestrial wireless IoT services such as LoRa [2] and Sigfox [3] for mountainous and marine areas.

Fig. 1 shows the structure of the satellite IoT system. In the satellite IoT communication system, the collecting station has a function of transmitting uplink feeder link data and collecting and processing responses from multiple terminal stations. A terminal station needs a low-power access protocol and miniaturization of the terminal station for IoT service. For this reason, an application-specific integrated circuit (ASIC) chip must be manufactured, and also a random multiple access protocol for multiple terminal stations must be supported. User uplink and downlink frequency is considered 400MHz and UHF band, respectively, and feeder uplink and downlink is considered S-band. This paper intends to deal with the terminal ASIC design method for a satellite IoT transmission.

In a satellite IoT system, it is necessary to consider several environments, such as LEO satellite constellation and terminal type, for operation. The scenarios for LEO satellite deployment are a full constellation and a partial constellation. Full constellation is a situation in which LEO satellite can support the entire globe, and partial constellation is a situation in which one or more LEO satellites are deployed, and a satellite IoT terminal cannot always access LEO satellites. In the type of a satellite IoT terminal, there is a case in which the terminal is with a GNSS receiver to know its location and absolute time information. In addition, the ephemeris information of the serving LEO satellite is known to the satellite IoT terminal in advance, and the visible time at which the terminal can see the LEO satellite is known to the terminal in some cases.

Depending on the satellite constellation and the IoT terminal type, four operation scenarios can be set. The

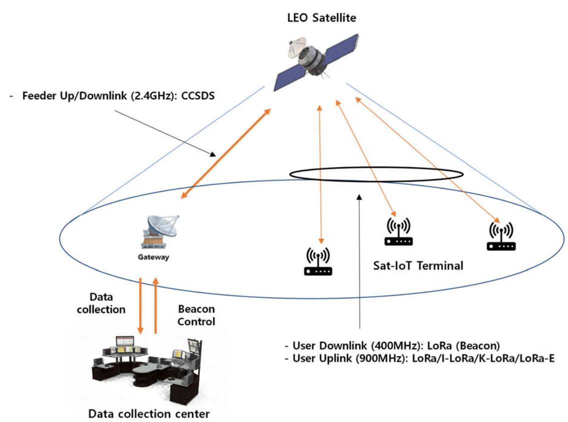

Fig. 1. Structure of the satellite IoT system

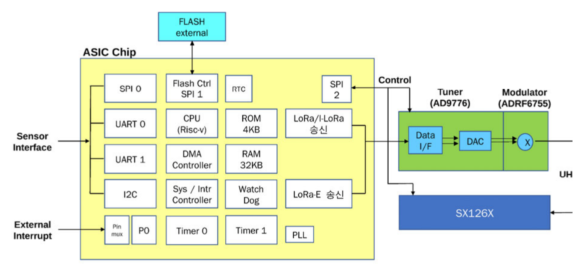

Fig. 2. Structure of terminal ASIC chip

advantages and disadvantages of each are summarized in Table 1. Although scenarios 1 and 2 are superior in terms of power and complexity, scenarios 3 and 4 are considered first in terms of actual implementation and operation.

TABLE I. OPERATION SCENARIOS

	Assumption	*Property*
Scenario1	Full constellation	- Simple - Terminal can transmit all the time - Low power consumption
Scenario2	Partial constellation & GNSS capability Preconfigured ephemeris information	- No need to receive beacon signals - Ephemeris information should be installed in USIM or memory
Scenario3	Partial constellation GNSS capability	Complex
Scenario4	Partial constellation	Simple

II. TERMINAL ASIC CHIP STRUCTURE

The structure of terminal ASIC chip is shown in Fig. 2. The external connection with the sensor, flash external, and tuner (AD9364) will be made centering on the ASIC chip. The data collected from the sensor is transmitted to the ASIC chip through the sensor interface, and the ASIC chip modulates the collected data into an uplink signal and sends it to the low earth orbit (LEO) satellite through the tuner. In addition, it also has a function to receive downlink beacon signals from LEO satellites, which plan to use LoRa-based signals and use a commercial SX126x chip developed by Semtech to process them. This device is designed to comply with the physical layer requirements of the LoRaWAN specification released by the LoRa Alliance.

ASIC chip consists of CPU, memory, DMA 4-channel, timer, sensor interface, and transmission block, and functions such as power save mode, package, MAC, and security algorithm must be implemented with software. In particular, the transmission function is the core block of the ASIC chip, and LoRa, I-LoRa, and LoRa-E transmission blocks will be implemented and installed.

Tuner must be able to transmit and receive uplink and downlink signals in UHF band, and plan to use AD9776 chip with DAC function inside. Memory is composed of the external flash controller, RAM for chip program and data memory, ROM for chip boot memory. DMA 4-channel is required for sensor interface module and LoRa transmission module. Timer is composed of the watch-dog for reset and interrupt and real time clock (RTC). Power save supports the Idle mode, sleep mode, and deep sleep mode.

III. SATELLITE IOT TRANSMISSION WAVEFORM

In the ASIC chip, three transmission waveforms, such as the LoRa, I-LoRa, and LoRa-E, will be used. LoRa, developed by Semtech, is a transmission technology using a chirp spread spectrum (CSS) waveform. It is strong against the Doppler effect and channel damage, but is vulnerable to multiple terminal interference [4]. Various spreading factors, which have the property of orthogonal transmissions, are provided to overcome the packet collisions. LoRa uses 8 preamble symbols for packet detection, a Hamming code for payload encoding, and a diagonal interleaver.

I-LoRa is a method developed by ETRI to improve the shortcomings of the existing LoRa [4]. The channel encoding method is changed to a convolutional code, and the bit-reversal method of the IEEE 802.15.4k standard is applied to the interleaver. In addition, the initial signal detection probability is increased by increasing the preamble length. In addition, two packets modulated with different spreading factors have orthogonality, and even if there is a section in which packet reception timings overlap in the same frequency band, they can be separately demodulated, so this is applied.

LoRa-E transmission is a transmission method based on frequency hopping, and it is a transmission method recently announced by Semtech to solve the weakness of existing LoRa to multiple terminal interference and to make it robust in a satellite transmission environment [5]-[8]. LoRa-E modem divides transmission data into blocks within a band to be used, performs frequency hopping in blocks and transmits them. The frequency bandwidth and center frequency used by each terminal are individually controlled for each terminal. The hopping frequency information used by the terminal is loaded in the header of the packet, and the gateway uses it to receive the packet. Each terminal may transmit a packet using a different center frequency and spreading bandwidth. When a plurality of terminals transmit data, a portion of the data divided into blocks may cause interference between terminals, resulting in a received data error. In order to recover such an error, the transmission data is error-correction-encoded, and the encoded data is interleaved and distributed in packets before transmission. A convolutional code is used for error correction coding, and the supported code rates are 1/3, 1/2, 2/3, and 5/6. Gaussian Minimum Shift Keying (GMSK) is used as the modulation method of the transmission signal.

IV. CONCLUSION

Through this study, we present an ASIC design method to secure terminal ASIC equipment with low speed, low power, and small characteristics to provide satellite IoT transmission service. The external connection with the sensor, flash external, and tuner will be made centering on the ASIC chip. Three transmission waveforms, such as the LoRa, I-LoRa, and LoRa-E, will be used to send the collected data to LEO satellite. As a result, the data collected from the sensor is transmitted to the ASIC chip through the sensor interface, and the ASIC chip modulates the collected data into an uplink signal and sends it to LEO satellite through the tuner.

ACKNOWLEDGMENT

This work was supported by Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (No.2020-0-00843, Development of low power satellite multiple access core technology based on LEO cubesat for global IoT service)

REFERENCES

[1] NSR, M2M and IoT via satellite, 7th Edition, 2017.

[2] Semtech, LoRa modem design guide: Sx1272/3/6/7/8, 2013, Available: https://www.semtech.com/

[3] Sigfox, Sigfox – The Golbal Communications Service Provider for the Internet of Things (IoT), 2018, Available: https://www.sigfox.com/

[4] S. Jung, G. Im, D.-H. Jung, P. Kim, J. G. Ryu, and J. Kang, *Performance analysis of DSSS- and CSS-based physical layer for IoT transmission over LEO satellites*, ETRI Journal (2022), 1–17. https://doi.org/10.4218/etrij. 2021-0038

[5] G. Boquet, P. Tuset-Peiro, F. Adelantado, T. Watteyne, and X. Vilajosana, LR-FHSS: Overview and Performance Analysis, IEEE Comm. Magazine, Vo. 59, Issue 3, Mar. 2021

[6] P. Kim, S. Jung, D. H. Jung, J. G. Ryu, and D. G. Oh, Performance Analysis of Direct Sequence Spread Spectrum Aloha for LEO Satellite Based IoT Service, IEEE 90th Vehicular Technol. Conf. (Honolulu, USA), 2019, pp. 1–5.

[7] A. Berni and W. Gregg, *On the Utility of Chirp Modulation for Digital Signaling,* IEEE Trans. Commun. **21** (1973), no. 6, 748–751.

[8] G. Ferré and A. Giremus, *LoRa Physical Layer Principle and Performance Analysis*, IEEE 25th Int. Conf. Electron. Circuits Syst. (Bordeaux, France), 2018, pp. 65–68.