A Ka-Band CMOS Beamforming Front-End IC for RF Inter Satellite Link System

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***Abstract*—A *Ka*-band CMOS 1-channel beamforming front-end IC for RF inter-satellite link system is presented. In particular, variable gain phase shifters (VGPS) and PA linearizer are integrated. The VGPS has an orthogonal phase and gain control function, which reduces chip size and power consumption. The PA linearizer reduces both AM-AM and AM-PM distortions of the PA, which improves linear output power. The 1-channel beamforming front-end IC has 6-bit phase and 6-bit gain control resolutions with TX OP_{1dB} of 18.5 dBm.**

***Keywords*—beamforming, CMOS, linearizer, orthogonal phase and gain control, phase shifter, receiver, transmitter**

I. Introduction

Beamforming technology is one of the key technologies for RF inter-satellite link systems. In particular, CMOS-based beamforming front-end ICs are receiving much attention due to their high level of integration and low cost [1]-[9]. However, CMOS PA has poor linearity and efficiency. Since the conventional digital pre-distortion is not easy to be applied to the phased array system [8], an analog PA linearizer must be integrated. Also, the conventional phase and gain control blocks have high phase and gain errors with large chip sizes. To solve these issues, a 1-channel CMOS beamforming front-end IC including PA linearizer and variable gain phase shifter (VGPS) with lower phase and gain error is proposed.

II. Proposed Beamforming Front-End IC

Fig. 1 shows the block diagram of the beamforming front-end IC. Each channel contains PA, PA linearizer, VGPS, T/RX switch, and LNA. All differential structures is adapted to reduce the parasitic ground inductance effect. A VGPS based on [10] is used for phase and gain control. To improve phase/gain control speed, short gate length transistors are used for the phase/gain control DAC. Fig. 2 shows the simulated static vector constellations of the 1-channel front-end IC. It can cover 360° with low gain errors.

The PA linearizer in [8], [12] improves both AM-AM and AM-PM distortion of the PA. However, its improvement in AM-PM distortion is very limited. Also, the linearizers lower the efficiency of the PA. To solve this issue, a two-stack Cold-FET-based linearized is proposed and connected to the input of the CS amplifier. Thanks to the proposed structure, AM-PM distortion is reduced and efficiency degradation due to the linearizer is minimized.

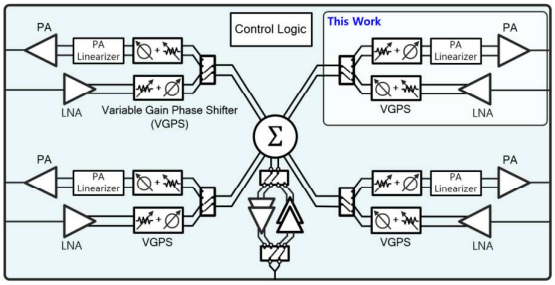

Fig. 1. Block diagram of the RF beamforming front-end IC.

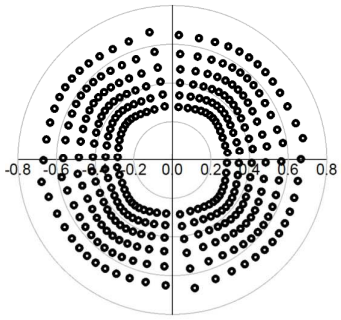

Fig. 2. Simulated static vector constellations of the 1 channel front-end IC at 26 GHz.

A differential SPDT structure with alternating NMOS and PMOS structure [11] is used for the T/RX switch to have high power handling capability with low insertion loss.

III. Implementation and Measurement Results

The proposed 1-channel beamforming front-end IC was fabricated using a 65-nm RF CMOS process. Fig. 3 shows a chip photo of the implemented 1-channel beamforming front-end IC. The IC was measured using on-wafer probing. Fig. 4 shows measured gain with respect to output power. Thanks to the analog linearizer, the gain is expanded in the high power region, which improves AM-AM distortion of the PA. OP_{1dB} of 18.5 dBm is achieved with the linearizer. Compared to that of the PA without the linearizer, OP_{1dB} of ~2.5 dB is improved. Fig. 5 shows a measured AM-PM distortion of the 1-channel IC. Thanks to the analog linearizer, the phase is lagged in the

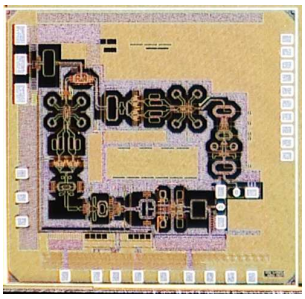

Fig. 3. Chip photo of the 1-channel beamforming front-end IC.

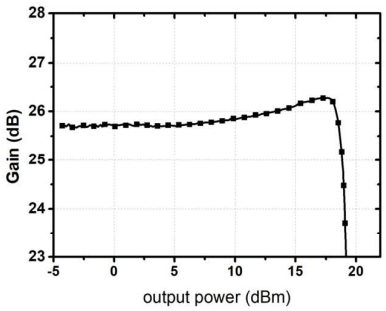

Fig. 4. Measured gain of the 1-channel beamforming front-end IC with respect to output power.

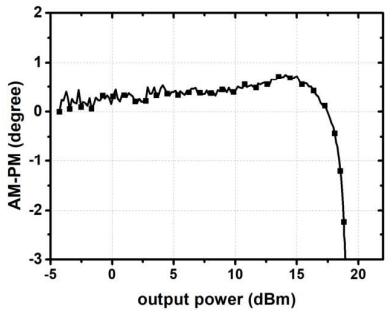

Fig. 5. Measured AM-PM distortion of the 1-channel beamforming front-end IC.

mid-power region and is led in the high-power region. The measured AM-PM distortion until OP_{1dB} was less than 1.5°. Compared to that of the PA without the linearizer, AM-PM distortion of about 3° is reduced. The RMS phase error was lower than 1.5° at 27 GHz.

IV. CONCLUSION

A *Ka*-band CMOS 1-channel beamforming front-end IC for RF inter-satellite link system was presented. The VGPS with an orthogonal phase and gain control function reduced chip size and power consumption. The Cold-FET-based linearizer reduced both AM-AM and AM-PM distortions of the PA with minimal efficiency degradation. Table Ⅰ shows the performance comparison with recently reported *Ka*-band Si-based beamforming front-end ICs. The proposed 1-channel IC achieved the highest OP_{1dB} and the lowest RMS phase and gain errors. It also has comparable NF and phase/gain control resolution.

TABLE I. PERFORMANCE COMPARISON WITH RECENTLY REPORTED KA-BAND BEAMFORMING ICS

Parameter	This Work	IBM JSSC17 [5]	Tokyo Tech. ISSCC 19 [6]	LG JSSC18 [3]	Qualcomm ISSCC18 [13]	UCSD JSSC18 [1]
Process	65 nm Bulk CMOS	130 nm SiGe BiCMOS	65 nm Bulk CMOS	28 nm LP CMOS	28 nm LP RF CMOS	180 nm SiGe BiCMOS
Tx OP1dB (dBm)	18.5	13.5	11.3	9.5	12	10.5
Phase/Gain Control Resolution (bit)	6 / 6	5 / 5	-	3 / -	3 / 3	6 / 4
RMS Phase Error by Phase & Gain Control (°)	< 2 (Phase & gain simultaneous control)	8** (gain control only) 1.5 (phase control only)	- / 1.8 (phase control only)	- / 7 (phase control only)	-	6** (gain control only) 5 (phase control only)
RMS Gain Error (dB)	< 0.2	1.4 **	0.4	-	-	0.9
Noise Figure (dB)	< 4 ***	6	4.2	6.7	3.8 *	4.6

* Estimated from the paper, ** Peak error, ***Simulation Result

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