Development of Filtered Low Noise Amplifier for Improving Antenna Signal Reception

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***Abstract*—This paper presents the development of a Low Noise Amplifier (LNA) integrated with filter for improving antenna signal reception to achieve a compact configuration for radio frequency (RF) receiver. The configuration, namely Filtered Low Noise Amplifier (FLNA), consists of an integrated single-layer transistor-based LNA circuit with a Bandpass Filter (BPF) constructed by Substrate Integrated Waveguide (SIW) technique. The proposed FLNA which is intended to operate at the center frequency of 2.4 GHz is designed and realized on a 1.6 mm thick Flame Retardant (FR) 4 epoxy dielectric substrate. The characterization results show that the realized FLNA has the –3 dB bandwidth response of 980 MHz (1.88 GHz–2.86 GHz) and the gain of 11.012 dB. These results are comparable to the simulated ones demonstrating the suitability for the desired RF application in improving antenna signal reception.**

***Index Terms*—Bandpass Filter (BPF); Filtering Low Noise Amplifier (FLNA); Low Noise Amplifier (LNA); Substrate Integrated Waveguide (SIW).**

I. Introduction

The demands for diverse wireless devices and services have led to a significant growth in wireless communication [1]. In order to fulfill specific requirements, it is necessary to ensure that RF applications is available to operate at their highest possible levels of efficiency. To satisfy these requirements, the devices in the RF receiver including filter, power divider, and LNA become essential parts and inseparable from the whole system. Numerous investigation related to the development of those parts have been carried out by many researchers [2]–[8]. The investigation to integrate some parts has also been focused to optimize the performance of RF receivers [3]. The integration between parts is usually expected to satisfy some specific requirements such as compact and lightweight, low production costs, ease of fabrication, and optimum performance.

On the receiving side of wireless communication system, a front-end amplifier, commonly using LNA, is among the most crucial part of RF receiver. This part is responsible to recover and amplify signal received by antenna from a transmitter. The antenna signal reception may be weak and contain noises and interferences. To provide detectable reception quality, the front-end amplifier must provide low noise figure, and sufficient power gain, so that the received signal is processable at the next level [5]– [8]. In the design of LNA as front-end amplifier, there are a number of design parameters involved, including linearity, impedance matching, and power dissipation as additional of noise figure and power gain [6]. Some methods for maintaining RF receiver stability have been implemented, including resistive impedance matching, balanced circuits, and negative feedback [7]. However, due to a variety of parameter, the reliability of its active components, such as transistors, is the single most critical aspect that should be given the highest priority. In addition, the LNA sometimes should fulfill other technical standards such as compact size, integrable with other part, and easy and lightweight construction [7]–[8].

The integration of LNA with other part, such as filter, enables in obtaining a compact front-end device. One of the techniques often used for realizing an integrated filter with LNA is Substrate Integrated Waveguide (SIW) technique [9]–[10]. Basically, SIW structure is made up of two rows of metal vias which are inserted in a metal-enclosed substrate. The technique has also been identified as a simple solution for incorporating non-planar waveguide structures into planar dielectric substrates [11]. Moreover, SIW is able to integrate different techniques to improve the performance of device [12]–[15]. The use of SIW structures in filter development is satisfiable the required specifications, particularly for filter with narrowband response [13]. Here, the SIW-based filters have a number of advantages, including an easy integration process, a high Q-factor, low cost, and compact size [14]–[15].

This paper proposes the integration of filter and LNA, namely Filtered Low Noise Amplifier (FLNA), to achieve a compact configuration for RF receiver. The proposed FLNA is intended to operate at the center frequency of 2.4 GHz and optimally work as a font-end device for improving antenna signal reception. The development of FLNA consists of a

BPF designed based on SIW technique and an LNA circuit configured using a transistor of BFP840ESD type [16]. The use of SIW technique is to ensure the successful integration of active and passive components on the same dielectric substrate [17]. An FR4 epoxy dielectric substrate with the thickness of 1.6 mm is used to realize the proposed FLNA based on the optimum design. The measured parameters of realized FLNA will be then compared with the ones obtained from the simulation for further discussion.

II. Overview of FLNA Design

As illustrated in Fig. 1, the proposed FLNA which aims to improve antenna signal reception consists of an SIW BPF and LNA. Prior being amplified by the LNA, the incoming signal received by the antenna is filtered first by the SIW BPF. In the filtering process, the bandwidth of incoming signal will truncated and limited by the cut-off frequencies of filter. The filtered signal is then passed through the transistor-based LNA circuit to be recovered and amplified due to the attenuated effect during the process of filtering. After passing through the LNA, the output signal is appropriate for further processes with the desired center frequency of 2.4 GHz.

A. Configuration of LNA Circuit

Fig. 2 depicts the proposed schematic LNA circuit which is mainly configured by using an RF bipolar junction transistor (BJT) of BFP840ESD type [16]. This transistor type is used due to its capability to operate with high performance at low current and voltage. The transistor is also workable at multi-band frequencies which cover the frequency of 2.4 GHz, hence, it is suitable for a front-end amplifier application. It shows that the circuit, at both input and output ports, possesses RF blocking capabilities in addition to the DC biasing and DC blocking components. Table I summarizes the value of each component for proposed LNA circuit which is determined after optimization during the design.

To achieve the appropriate gain and quiescent point, at first, the value of DC-bias related components is calculated for optimization, and then put the LNA circuit for DC analysis to acquire the values for R_0, R_1, R_2, R_3, and R_4. When calculating the value of L_1 and L_2 which are connected to the transistor, it is necessary to take into account the frequency of the power supply that may cause interference with the RF signal. It is

TABLE I
VALUE OF EACH COMPONENT FOR LNA CIRCUIT.

Symbol	*Value*	*Symbol*	*Value*
R_0	0 Ω	L_1	2.7 nH
R_1	10 Ω	L_2	2.7 nH
R_2	30 kΩ	C_1	3.9 pF
R_3	82 Ω	C_2	4.7 pF
R_4	10 Ω	C_3	39 pF
		C_4	39 pF

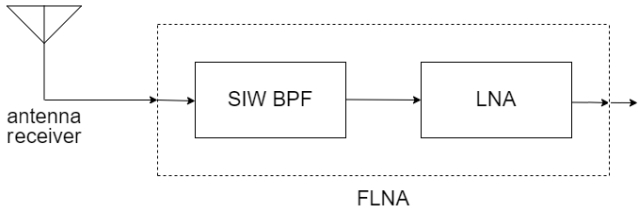

Fig. 1. Block diagram of FLNA for improving antenna signal reception.

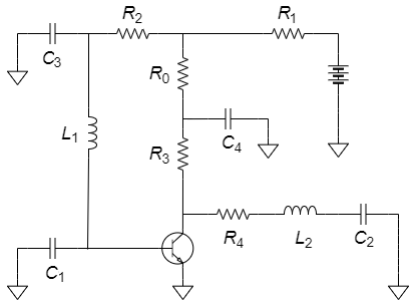

Fig. 2. Proposed schematic LNA circuit.

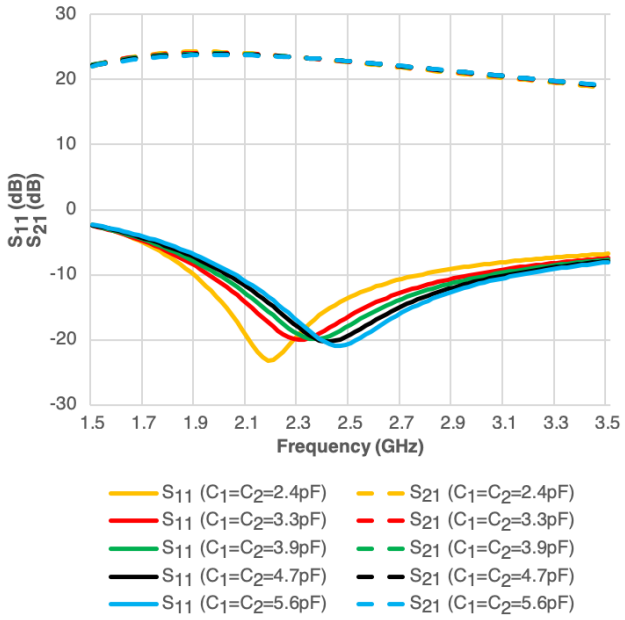

Fig. 3. Simulated return loss and gain for proposed LNA circuit.

noted that L_1 and L_2 are connected to the transistor to prevent the RF signal from the power supply coming to the circuit and vice versa. This can be accomplished by connecting L_1 and L_2 leads to the transistor. The DC current in the circuit is then blocked by using C_1 and C_2. The frequency of RF signal is one factor that can be considered since it can interfere the DC power supply. Therefore, the values of C_3 and C_4 should be determine to smooth the DC power supply and avoid noise from the RF signal. According to the application note, the proposed LNA circuit in such configuration is able to generate a power gain more than 19 dB. In order to achieve the required gain, the transistor need the DC power supply with I_{CC} of 10 mA and V_{CC} of 3 V. Meanwhile, both the input and output impedances are designed to have Z_0 of 50 Ω.

Based on the calculated values for each component and transistor parameter, the proposed LNA circuit is simulated using a simulation software. Fig. 3 plots the simulated return loss (S_{11}) and gain (S_{21}) for the proposed LNA circuit. The values of S_{11} and S_{21} are taken for varied values of capacitor at the input and output ports, i.e., C_1 and C_2, as the most significant components among others, in order to obtain the optimum result. It shows that the value of 4.7 pF for both capacitors, the proposed LNA circuit has the highest performance at the frequency of 2.4 GHz with the gain achievement of 22.59 dB.

B. Configuration of SIW BPF

The fundamental architecture of SIW structure is basically constructed by two rows of metal vias which are inserted in a metal-enclosed substrate. These two rows of metal vias are applied to connect the groundplane on bottom side of the structure to the SIW surface or patch on top side of the structure. The diameter of the metal vias, the distance between the centers of two adjacent vias (pitch), and the width of SIW surface are all important physical elements of the SIW structure. The low frequency signal is not allowed to propagate through the SIW structure, as this will cause it to generate a particular cut-off frequency. This is similar to a conventional waveguide due to the fact that it contains two rows of metal vias that serve as side walls.

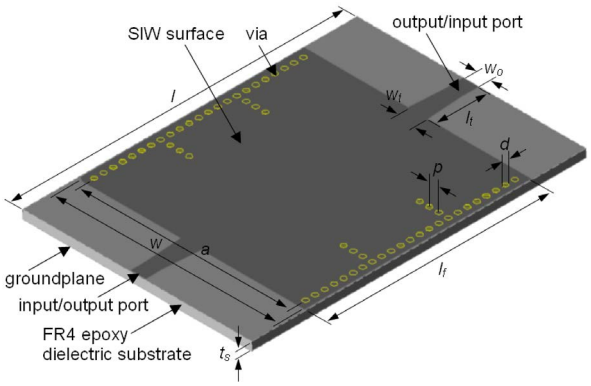

Fig. 4. Configuration of proposed SIW BPF

TABLE II
GEOMETRY VALUE OF SIW BPF.

Parameter	*Value*	*Parameter*	*Value*
l	60 mm	l_f	43 mm
w	43 mm	a	40 mm
l_t	8.5 mm	p	1.8 mm
w_t	4 mm	d	1 mm
w_o	3 mm	t_s	1.6 mm

Fig. 4 shows the configuration of proposed SIW BPF designed to have the center frequency of 2.4 GHz. The configuration is deployed on an FR4 epoxy dielectric substrate with the thickness (t_s) of 1.6 mm. There are 23 metallic vias that serve to make three SIW cavities. To achieve the values of return loss (S_{11}) and insertion loss (S_{21}) having good response while yet maintaining its sufficient bandwidth, the partition of three SIW cavities is carried out using a ratio of 1:1:1. The SIW cavity, as the basic constituent of the filter, is actually an open structure due to the radiating space between vias resulting in power leakage loss [18]. The width of SIW surface (a) is 40 mm, while the diameter of metallic via (d) and the pitch (p) are 1 mm and 1.8 mm, respectively. Other geometry values of the proposed SIW BPF are tabulated in Table II obtained from the optimization.

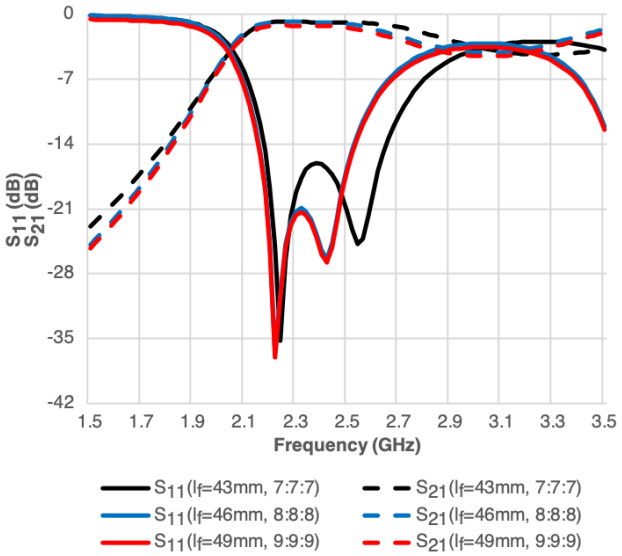

Fig. 5. Simulated return loss and insertion loss for SIW BPF.

Fig. 5 plots the simulation results of return loss (S_{11}) and insertion loss (S_{21}) for the proposed SIW BPF with varied value of SIW surface length (l_f). It shows that the proposed SIW BPF with the l_f value of 43 mm yields the optimum result with the –3 dB bandwidth response of 1.15 GHz (2.03 GHz–3.18 GHz). The configuration achieved the values of S_{11} and S_{21} of –16.208 dB and –0.889 dB at the center frequency of 2.4 GHz, respectively, which can satisfy the desired application.

C. Integration of SIW BPF and LNA

Fig. 6 illustrates the integration of SIW BPF and LNA yielding a compact FLNA configuration. All parts are designed and deployed on an FR4 epoxy dielectric substrate with the thickness of 1.6 mm. The via position is along the SIW surface with the diameter (d) of 1 mm and the pitch (p) of 1.8 mm. The SIW BPF and LNA are connected each other using a tapered microstrip feeding line with the length of 3 mm. The use of tapered microstrip feeding line is to acquire an impedance match between both parts. The tapered microstrip feeding line has the width of 4 mm at the SIW side (w_t) and 3 mm at the other side (w_o). Table III depicts the geometry value of proposed FLNA for the realization.

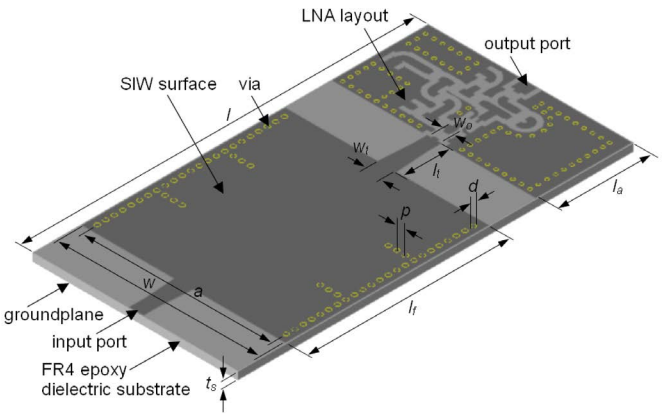

Fig. 6. Configuration of FLNA as integration of SIW BPF and LNA.

TABLE III
GEOMETRY VALUE OF FLNA.

Parameter	*Value*	*Parameter*	*Value*
l	83.25 mm	l_f	43 mm
w	43 mm	a	40 mm
l_t	8.5 mm	p	1.8 mm
w_t	4 mm	d	1 mm
w_o	3 mm	t_s	1.6 mm
		l_a	20.27 mm

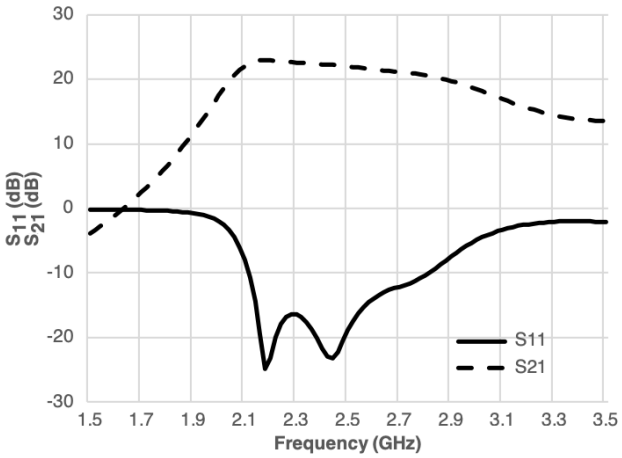

Fig. 7. Simulated return loss and gain for FLNA.

In order to achieve a compact FLNA configuration, the LNA circuit is designed to employ surfaced-mount device (SMD) for all passive components. A transistor of BFP840ESD type is used to obtain gain of more than 19 dB at the frequency of 2.4 GHz with value of noise figure of 1.14 dB. It should be noted that there are several parameters of R, L, and C designed as DC blocking, DC biasing, input and output impedance match, and gain adjustment. According to the application note, the transistor has good stability in its operation frequency where the parameter values at the frequency of 2.4 GHz are S_{11} of 0.067∠–138.416°, S_{12} of 0.026∠92.835°, S_{21} of 14.313∠–148.912°, and S_{22} of 0.259∠–165.291°.

Fig. 7 plots the simulated return loss (S_{11}) and gain (S_{21}) for the proposed FLNA. It shows that the values of S_{11} and S_{21} at the frequency of 2.4 GHz are value is –21.670 dB and 23.311 dB, respectively. Meanwhile, the –3dB bandwidth response of proposed FLNA is around 1.08 GHz (2.04 GHz–3.12 GHz) covering the center frequency of 2.4 GHz, in which the achievement results are adequate for improving antenna signal reception of RF receiver.

III. REALIZATION, CHARACTERIZATION, AND RESULT COMPARISON

A. Characterization of SIW BPF

Fig. 8 depicts the realized SIW BPF, as part of FLNA, for experimental characterization. An FR4 epoxy dielectric substrate with the thickness of 1.6 mm is applied for the deployment using a wet etching technique. Two 50 Ω SMA connectors are attached at each port of realized SIW BPF to measure its parameters including return loss (S_{11}) and insertion loss (S_{21}). The measurement results are then compared with the ones from simulation for further analysis.

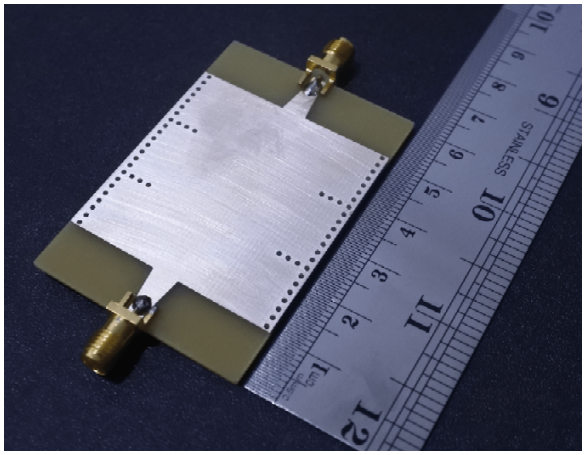

Fig. 8. Picture of realized SIW BPF for experimental characterization.

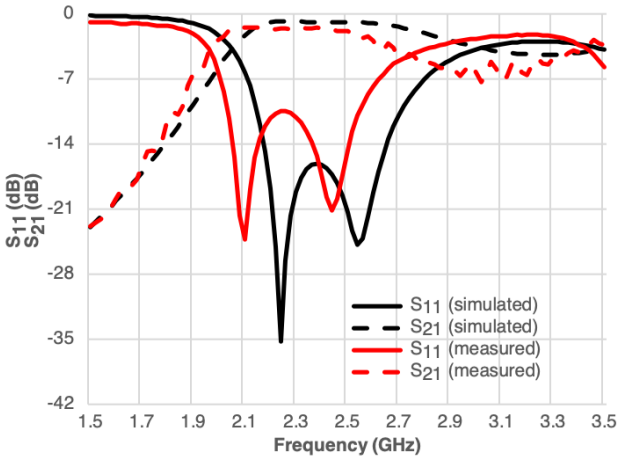

Fig. 9. Comparison of measured and simulated results for SIW BPF.

The comparison of measured and simulated results is plotted in Fig. 9 which demonstrates the trend of agreement qualitatively between the results with some discrepancies in their frequency response and magnitude. The frequency response of measured results is shifted compared to the simulated ones, while the magnitude is becoming worse around the center frequency of 2.4 GHz. These discrepancies are mostly affected by the different parameter values of FR4 epoxy dielectric substrate, i.e., dielectric constant and dielectric loss. The lower dielectric constant affects to the shift of frequency response, while the worse dielectric loss influences the magnitude. Furthermore, the –3dB bandwidth response of realized SIW BPF is around 980 MHz (1.93 GHz–2.91 GHz). This result is 170 MHz narrower than the simulated one which also possibly evoked by the dielectric loss of FR4 epoxy dielectric substrate used in the realization.

B. Characterization of FLNA

Similar to the realized SIW BPF, implementation of the proposed FLNA also employs an FR4 epoxy dielectric substrate with the thickness of 1.6 mm. The manufacture process for realizing the proposed FLNA is carried out using a wet etching technique. Fig. 10 shows the realized FLNA with two 50 Ω SMA connectors attached at the input port of LNA and the output port of SIW BPF, respectively. To achieve a compact configuration of realized FLNA, SMD components are implemented for all resistors, inductors, and capacitors of LNA. Experimental characterization is performed to measure parameters of FLNA including return loss and gain.

The results of experimental characterization are then compared to the simulated ones as plotted in Fig. 11. It shows that

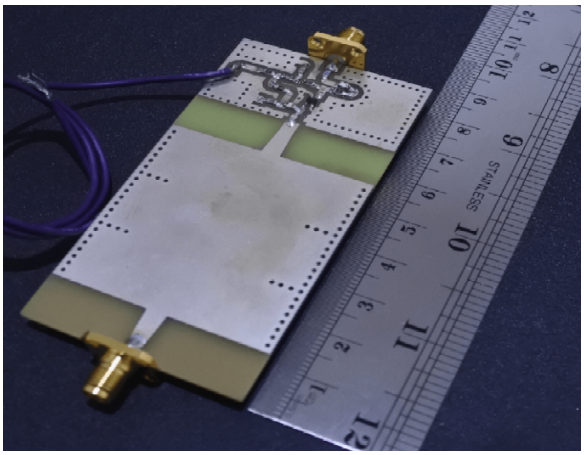

Fig. 10. Picture of realized FLNA for experimental characterization.

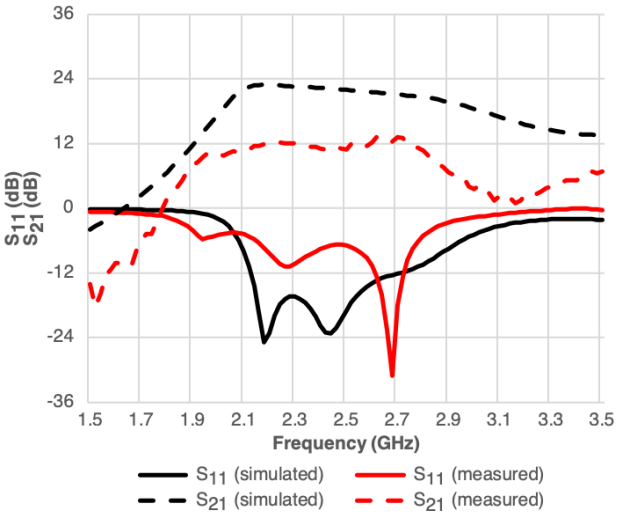

Fig. 11. Comparison of measured and simulated results for FLNA.

the measurement of realized FLNA has the similarity in trend with some discrepancies to the simulation. The measured –3 dB bandwidth response achieved 980 MHz (1.88 GHz–2.86 GHz) which was 100 MHz narrower than the simulated result. At the frequency of 2.4 GHz, the measured return loss (S_{11}) and gain (S_{21}) are –7.595 dB and 11.012 dB, respectively. In general, the measured results are worse than the simulated ones, in particular, around the center frequency of 2.4 GHz. These facts are similar to the measurement of realized SIW BPF, in which the different parameter values of dielectric substrate used for the realization mainly influence the measured results. Meanwhile the different parameter values of transistor as an active component for amplification is to be another issue affecting the gain achievement of FLNA lower than the simulation. Nevertheless, the realized FLNA is still adequate to amplify the antenna signal reception.

IV. Conclusion

The development of FLNA as an integration of LNA and SIW BPF for improving antenna signal reception has been presented. The LNA has been designed and powered using an RF transistor of BFP840ESD type, while the filter was implemented by SIW technique. The proposed FLNA was deployed on an FR4 epoxy dielectric substrate with the thickness of 1.6 mm. The characterization results showed that the measurements of FLNA have some discrepancies in the performance compared to the simulations. The realized FLNA has the –3 dB bandwidth response of 980 MHz which was 100 MHz narrower than the simulated result, while the S_{11} and S_{21} values at the frequency of 2.4 GHz are –7.595 dB and 11.012 dB, respectively. In addition, a further investigation is still in progress to improve the performance of FLNA to be more suitable for the desired application.

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