

A Novel Interleaving Scheme for Concatenated Codes on Burst-Error Channel

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Abstract—With the rapid development of Ethernet, RS (544, 514) (KP4-forward error correction), which was widely used in high-speed Ethernet standards for its good performance-complexity trade-off, may not meet the demands of next-generation Ethernet for higher data transmission speed and better decoding performance. A concatenated code based on KP4-FEC has become a good solution because of its low complexity and excellent compatibility. For concatenated codes, aside from the selection of outer and inner codes, an efficient interleaving scheme is also very critical to deal with different channel conditions. Aiming at burst errors in wired communication, we propose a novel matrix interleaving scheme for concatenated codes which set the outer code as KP4-FEC and the inner code as Bose-Chaudhuri-Hocquenghem (BCH) code. In the proposed scheme, burst errors are evenly distributed to each BCH code as much as possible to improve their overall decoding efficiency. Meanwhile, the bit continuity in each symbol of the RS codeword is guaranteed during transmission, so the number of symbols affected by burst errors is minimized. Simulation results demonstrate that the proposed interleaving scheme can achieve a better decoding performance on burst-error channels than the original scheme. In some cases, the extra coding gain at the bit-error-rate (BER) of 1×10^{-15} can even reach 1 dB.

Index Terms—Error correcting codes (ECC), concatenated codes, Reed-Solomon(RS) code, interleaving scheme, burst-error channel

I. INTRODUCTION

Recently, the continuous growth of computing-intensive workload and the steady maturity of network infrastructure technology promote the persistent upgrading and development of Ethernet. The early transmission rate specified for Ethernet was only 2.94 Mb/s, but in just a few decades, it has increased to hundreds of Gb/s [1]–[3]. At the same time, the requirement of Ethernet for higher performance is becoming more and more urgent. RS(544, 514) called KP4-forward error correction (FEC) [3], [4] is widely used in high-speed Ethernet because of its proper complexity, low latency, acceptable performance, and good adaptability, while it is hard for RS(544, 514) with limited coding gain to meet the performance requirements of the next-generation Ethernet as the transmission rate increases.

There are two options to solve this problem. One is to increase the code length of a single FEC code. However, this way is inefficient because the computational complexity will grow exponentially with the increase of codeword length. Another option is concatenated codes which can attain high performance with acceptable computational complexity due to

its special structure and flexibility to choose inner and outer codes. Therefore, proper concatenated codes could be a better choice than a powerful but longer single code.

Concatenated codes are constructed with two or more codes in order to achieve good performance while maintaining low complexity. Forney firstly introduced the concept of concatenated codes in 1965 [5]. In the past, more attention was focused on the selection of inner code and outer code [6]. Actually, choosing a reasonable interleaving method between the inner and outer codes can further improve the performance. Therefore, when applying concatenated codes to Ethernet communication, we should also comprehensively consider the channel conditions to design an appropriate interleaving scheme, which has not been discussed in detail before.

In the actual communication channels, errors caused by interference are often in series which are called burst errors [7]–[10]. Burst errors often occur in wired and wireless communication, which will degrade the decoding performance obviously. By inserting an effective interleaving scheme between the inner and outer codes, the ability of concatenated codes to resist burst errors can be greatly improved. In this paper, we propose a novel interleaving scheme for the existing RS-BCH concatenated FEC scheme, which will facilitate better performance on burst-error channels in the next-generation Ethernet applications.

II. PRELIMINARIES

A. RS Codes and BCH Codes

RS code is the abbreviation of Reed-Solomon code that is constructed in the Galois field $GF(2^m)$ [11]. RS (n, k) codes are a class of linear block codes, in which n and k indicate the codeword symbol length and information symbol length, respectively. Each symbol contains m number of bits [12]. Given a symbol size m , the maximum codeword length for an RS code is $n = 2^m - 1$, but it may be shortened by setting some information symbols to be zero at the encoder which means the length of RS codes can be $n < 2^m$. The RS encoder generates $2t = n - k$ parity symbols, where t means the correction capability. RS code is an error correcting code (ECC) decoded in symbol that makes it especially suitable for correcting burst errors. No matter how long the length of the burst error is, as long as these error bits are all in the same symbol, it is just one error for RS code.

Similarly, Bose-Chaudhuri-Hocquenghem (BCH) codes are another type of linear block codes and can be defined using generator polynomials. Compared with RS code, BCH code is an ECC decoded in bit which is not so suitable for dealing with burst errors. However, its encoding and decoding processes are made simpler than those of RS codes because of its binary property. In addition, BCH codes perform better than RS codes with similar code rate and code length over the Additive White Gaussian Noise (AWGN) channel [13].

B. Concatenated Codes

Forney firstly proposed the concept of concatenated codes which use shorter codes to construct a long code in series or parallel in 1965 [5]. Single code can improve its performance by increasing the code length with growing complexity. Compared with single code, concatenated code could meet specific performance requirements with a reasonable decoding complexity.

The overall structure of a two-stage concatenated code is shown in Fig. 1. Because the outer code is directly related to the physical layer (PL), we can keep the PL unchanged if we set the outer code as a popularly used code in the present Ethernet standard. According to the latest report in the IEEE Std 802.3 in 2018 [3], two RS FECs, RS(528, 514) (KR4-FEC) and RS(544, 514) (KP4-FEC), were used in the sublayer. In our experiments, we choose concatenated code with KP4-FEC as the outer code and BCH as the inner code.

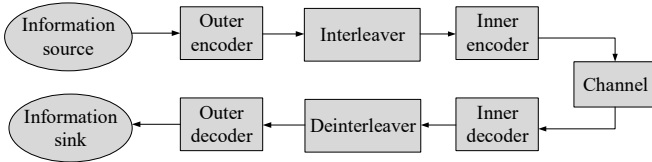


Fig. 1. The overall structure of a two-stage concatenated code.

III. THE PROPOSED INTERLEAVING SCHEME

Recently, the concatenated code consisting of 2 KP4-FECs as the outer codes and 80 BCH(144, 136) codes as the inner codes is proposed for Ethernet [14]. The specific coding scheme is as follows. After being encoded by the RS encoders, the two RS codes are interleaved at the symbol level as in Fig. 2. Symbols Ra_0, \dots, Ra_{543} come from RS code A and symbols Rb_0, \dots, Rb_{543} constitute RS code B, respectively. Then those messages are evenly divided into 80 frames which are going to be transmitted to the BCH encoders for the next encoding. Finally, the encoded BCH codes enter the channel in sequence.

The existing interleaving minimizes the number of symbols affected by continuous errors by maintaining the continuity of bits in each RS symbol when burst errors occur. It fully considers the characteristics of RS code that it is an ECC in symbol but ignores that BCH code is decoded in bit in which continuous errors have a disastrous impact on its decoding performance, especially the inner code is BCH(144, 136) with $t = 1$. The existing interleaving scheme will lead to decoding

failure or even miscorrection for BCH code in case of burst errors.

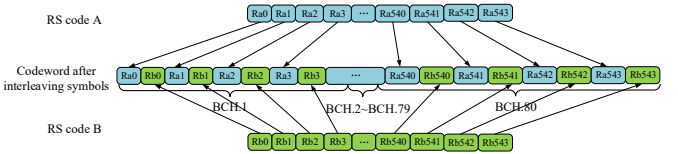


Fig. 2. Existing interleaving scheme.

Based on the above analysis, we come up with an interleaving idea which writes the RS encoded information into the matrix by column, then encodes them by row, and finally transmits them in column order to the channel. Through this operation, burst errors can be dispersed into multiple BCH codes at different intervals on the premise of ensuring the integrity of each symbol in RS codes. The length of the interval is decided by the width of column. Depending on the actual situation, different values can be set for the column width. The specific process is introduced as below.

First of all, we introduce the matrix representation of symbol as shown in Fig. 3. The w is the column width and we write the m (m is the symbol size of RS code) bits of every RS symbol into their matrix representations by row. This matrix representation is also the basic unit for interleaving. Our proposed matrix interleaving scheme can be divided into three steps. For the convenience of expression, it is assumed that the outer codes contain x RS codes and the inner codes contain y BCH codes.

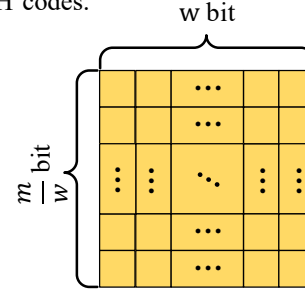


Fig. 3. Matrix representation of symbol.

As illustrated in Fig. 4(a), the first step is to preprocess the x encoded RS codes to make the remaining errors after BCH decoding can be evenly distributed into x RS codes. Odd numbered parts, e.g. *part.1*, are arranged in the order of RS.1 to RS. x , and even numbered parts, e.g. *part.2*, are arranged in the order of RS. x to RS.1, which make preparation for *Step 2*. The part length depends on the number of BCH decoders y and the column width w . The specific relationship can be described in equation (1):

$$part_length = \begin{cases} \frac{y \cdot w}{m} & , \frac{m}{w} \bmod y = 0; \\ \frac{lcm(y, \frac{m}{w})}{m} & , \frac{m}{w} \bmod y \neq 0, \end{cases} \quad (1)$$

where lcm refers to the least common multiple and $part_length$ is counted in symbol. Sometimes, the total number of symbols from x RS codes cannot be divided by $part_length$ and we use the remainder of them to form the last part *Part.n*.

Secondly, as Fig. 4(b) shows, we write the obtained sequence into a matrix in column order and encode the information matrix by row. It is worth noting that we use the matrix representation of symbols when writing information. Because the length of $Part.n$ may not be equal to $part_length$, we can cut its column width w to an appropriate value to make it adapt to the matrix. The same is true for the channel transmission in the third step in Fig. 4(c). In Fig. 4(b), we can find exchanging the order of RS codes every part length in *Step 1* makes the number of bits from every RS code almost equal for each BCH encoder in *Step 2*.

Thirdly, we use the method in Fig. 4(c) to transmit the encoded matrix. In each symbol matrix, bits are transmitted in row order while in each part, symbols are transmitted in column order. Through such a transmission mode, when burst error occurs, the continuous error is dispersed to multiple BCH codes. However, for RS code, the bits in each symbol are still centralized so that the error is less likely to be spread to other symbols.

In our experiments, considering boundary conditions, we set the column width w to 1 bit and 1 symbol (m bits). Meanwhile, we also consider $w = 2$ bits because 4 Pulse Amplitude Modulation (PAM4) is usually adopted in KP4, which transmits the codeword with 2 bits as 1 signal.

1) $w = 1$ bit

When we set w to 1 bit, the matrix widens the distance between adjacent bits to the greatest extent. Take the first BCH code as an example, it is hard for burst errors whose length is less than $part_length$ to affect its decoding performance because the error bits cannot be in the same BCH decoder in this situation.

2) $w = 1$ symbol (m bits)

Considering a special case that the error propagation of burst errors in the channel is not serious or even close to none like AWGN channels, there is no need to spread all the bits in each symbol across different BCH codes to resist the effects of continuous errors and a proper concentration of bits in each symbol can facilitate the decoding of RS codes. Compared with $w = 1$ bit, $w = 1$ symbol is set to separate adjacent symbols far away for burst errors which involve multiple symbols, while not to separate adjacent bits in one symbol. Although $w = 1$ symbol scheme as a symbol-level scheme cannot disperse the error bits as the $w = 1$ bit scheme, it can bring benefits to RS decoding.

In this design, as long as a BCH code is decoded successfully, all the symbols contained in it are correct. However, in $w = 1$ bit scheme, for a symbol to be completely correct, all m BCH codewords corresponding to the m bits in one symbol should be decoded correctly. Therefore, $w = 1$ symbol scheme can help achieve a better performance for channels with few burst errors.

3) $w = 2$ bits

Given the transmission characteristics of PAM4, it is rarely possible to for 2 bits of 1 signal to be both wrong at the same time when an error occurs. From this perspective, setting $w = 2$ bits will be enough to separate adjacent bits in 1

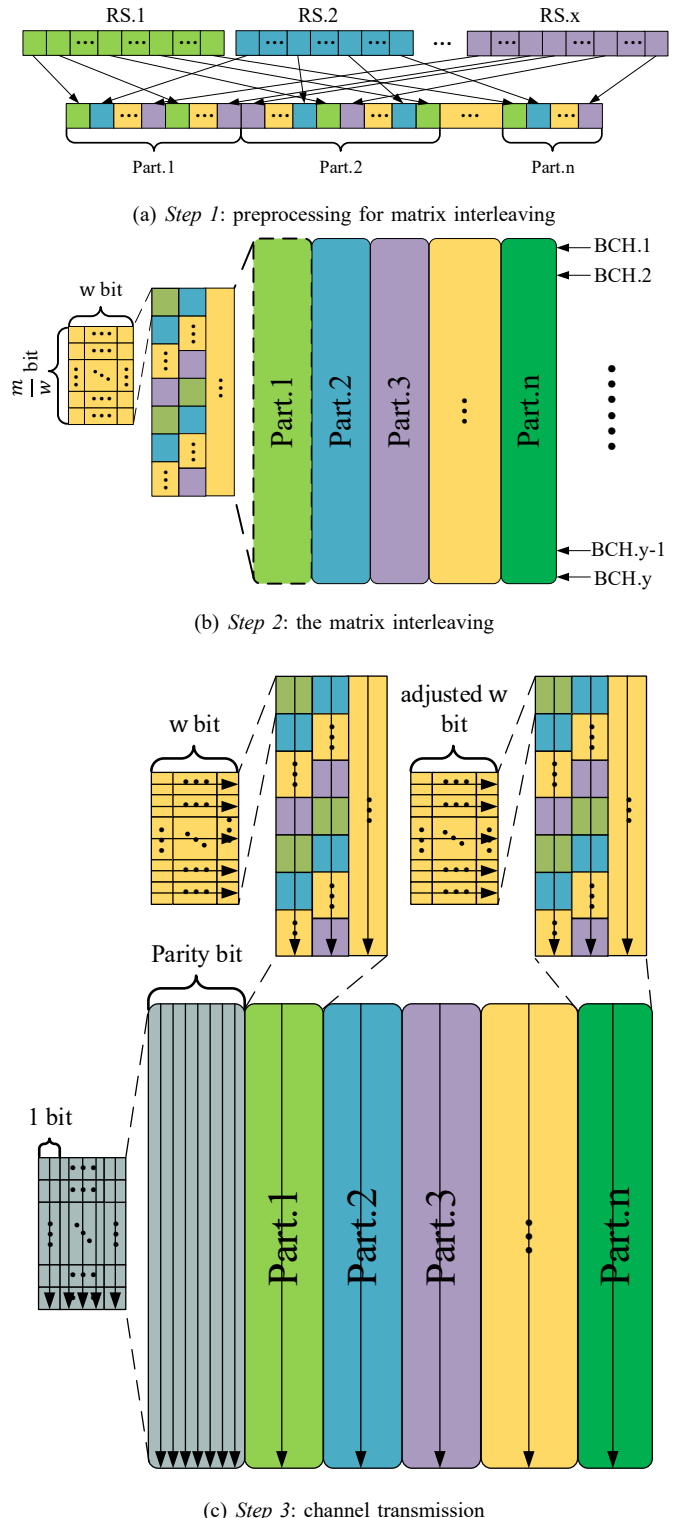


Fig. 4. The proposed matrix interleaving scheme.

symbol for BCH decoding, even comparable to the $w = 1$ bit scheme. While at the same time, compared with $w = 1$ bit, this setting increases the degree of bit concentration, which has a certain promotion effect on RS decoding. As a result, in terms of theoretical analysis, the $w = 2$ bits scheme could give a better performance than $w = 1$ bit on burst-error channels

with PAM4.

IV. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

In this section, simulation results and further performance analysis for the proposed interleaving scheme with different w compared with the existing interleaving scheme are shown in Figs. 5, 6, 7 and 8. For performance comparison with the existing scheme, the number of RS codes x and BCH codes y are set to 2 and 80, respectively. However, our proposed interleaving scheme is not limited to this, it can be extended to other similar concatenated codes that choose other codes to be inner and outer codes.

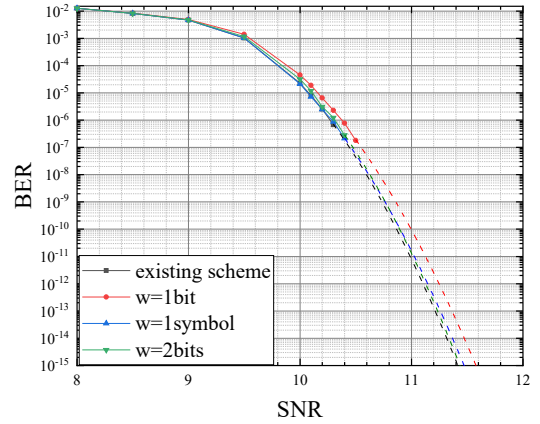
Concatenated codes with these interleaving schemes all use 2 KP4-FECs as the outer codes and 80 BCH(144, 136) codes as the inner codes, so they share the same data rate 0.89. The codeword is modulated by PAM4 and transmitted over AWGN channels and burst-error channels. The p in Figs. 5 and 6 is error propagation probability which represents the probability that the next signal will be wrong when the current received signal fails to transmit correctly. We apply one-tap Decision Feedback Equalizer (DFE) to model the error propagation process of burst errors, which convolves the PAM4 modulated symbols before adding AWGN and then uses DFE to recover the symbols in the receiver.

A. Simulation Results

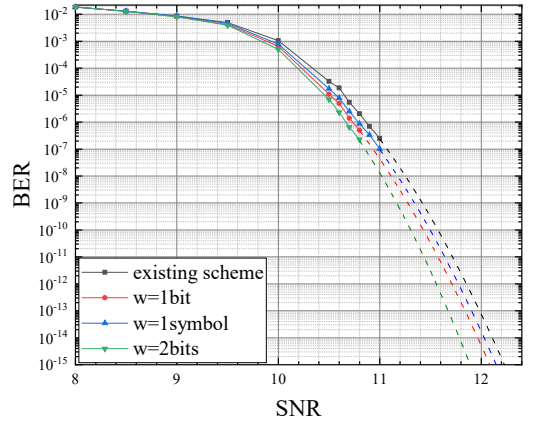
Our simulation reaches the BER of 1×10^{-7} , and then we observe the performance gap at the BER of 1×10^{-15} by fitting the curve.

In Fig. 5, we use BCH(144, 136) with hard decoding on the two different channels and set p as 0.3 and 0.75. When p is too large, like 0.75, the performance of all four interleaving schemes decreases seriously. Based on the characteristics of one-tap DFE, we add precoding to all schemes to resist burst errors for better performance. It can be observed from Fig. 5 that with the increase of p , our proposed interleaving scheme with different w always outperform the existing interleaving scheme on burst-error channels. When p is 0.75, the extra coding gain of the proposed matrix scheme is even up to 1 dB compared with the existing interleaving scheme. However, on AWGN channels with very few continuous errors, the $w = 1$ bit scheme is too fragmented, causing a certain degree of performance loss compared with existing interleaving schemes. Meanwhile, the $w = 1$ symbol and $w = 2$ bits schemes benefit from the integrity of the bits in each RS symbol in BCH codes to maintain their performance consistent with existing schemes, in which negligible performance loss can be found.

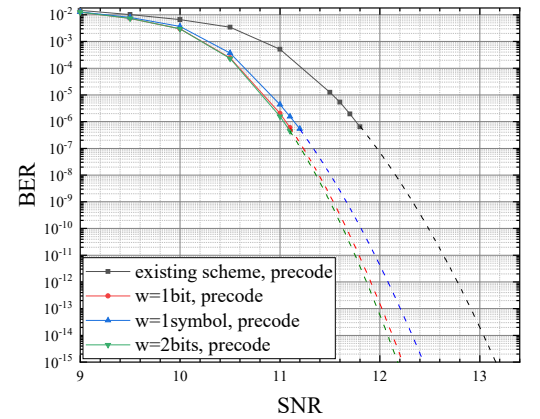
Then, we choose BCH soft decoding with stronger decoding ability for simulation, and the results are shown in Fig. 6. We consider the performance of the four interleaving schemes at BER of 1×10^{-15} when the number of flip bits is set to 3 ($F3$) in chase decoding. From Fig. 6(b), when $p = 0.3$, the $w = 1$ bit/1 symbol/2 bits schemes can get 0.32 dB/0.19 dB/0.44 dB extra coding gain, respectively. Then we use a larger p which is set to 0.5, the coding gain of $w = 1$ bit/1 symbol/2 bits schemes also get to 0.38 dB/0.14 dB/0.47 dB as in Fig. 6(c).



(a) AWGN



(b) $p = 0.3$

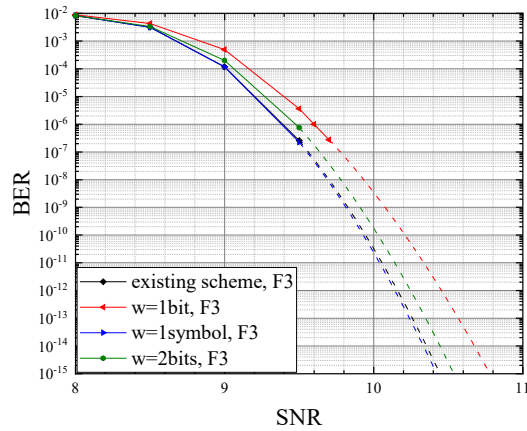


(c) $p = 0.75$

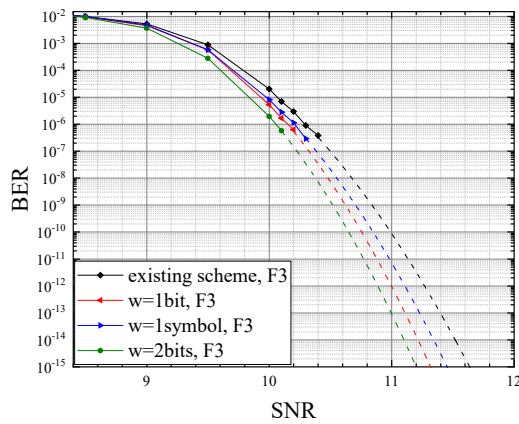
Fig. 5. Comparison of four interleaving schemes using BCH(144,136) hard decoding on a) AWGN channel; b) burst-error channel with $p = 0.3$; c) burst-error channel with $p = 0.75$.

B. Performance Analysis

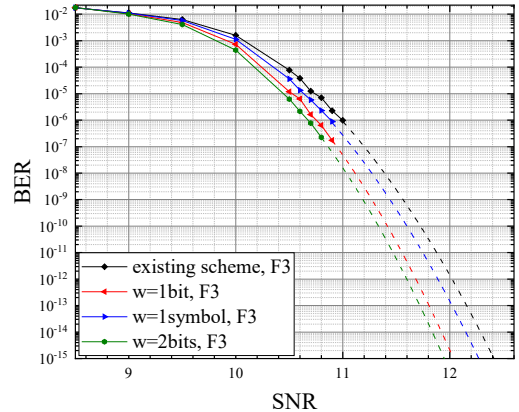
In addition, after simulating the overall performance of concatenated codes with different interleaving schemes, we intercepted the performance of BCH decoding in the concatenated codes to observe the effect of different interleaving schemes on the inner and outer codes of concatenated codes respectively, as shown in Figs. 7 and 8.



(a) AWGN, F_3



(b) $p = 0.3, F_3$

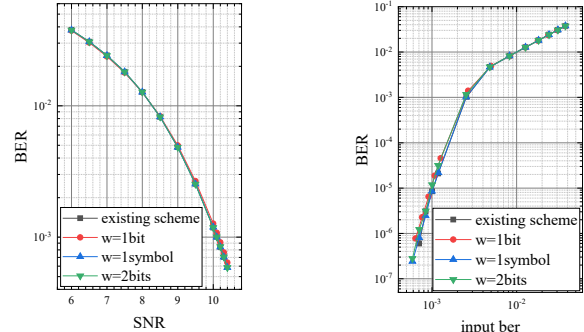


(c) $p = 0.5, F_3$

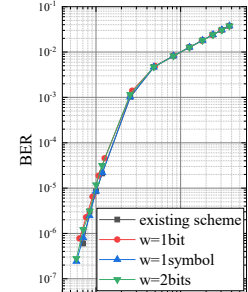
Fig. 6. Comparison of four interleaving schemes using BCH(144,136) soft decoding on a) AWGN channel, F_3 ; b) burst-error channel with $p = 0.3, F_3$; c) burst-error channel with $p = 0.5, F_3$.

Fig. 7 shows the simulation results on AWGN channels. We can find that whether using BCH hard or soft decoding, the decoding performance of BCH in existing scheme and $w = 2$ bits/ 1 symbol schemes is almost the same. However, BCH decoding of $w = 1$ bit scheme has some performance loss compared to the other three schemes and this loss is exacerbated when we replace the BCH hard decoding with soft

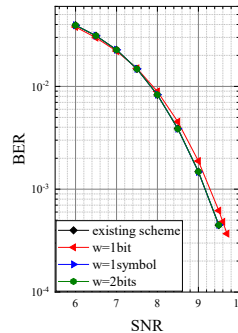
decoding. For RS decoding, on the whole, the two schemes at the bit level ($w = 1$ bit and $w = 2$ bits) and the two schemes at the symbol level (existing scheme and $w = 1$ symbol) remain consistent respectively, and obviously the dispersion of bits within the symbol brought by bit-level interleaving affects the decoding performance of RS codes to a certain extent.



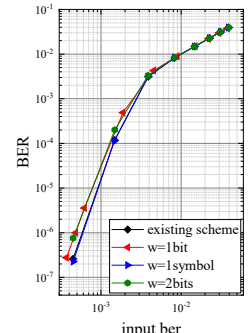
(a) HD, BCH



(b) HD, RS



(c) SD, F_3 , BCH



(d) SD, F_3 , RS

Fig. 7. BCH and RS decoding performance of four interleaving schemes on AWGN channels a) HD, BCH; b) HD, RS; c) SD, F_3 , BCH; d) SD, F_3 , RS.

Then, we turn to the burst-error channels and show the results in Fig. 8. It can be seen that on burst-error channels, although the bit-level interleaving is still inferior to the symbol-level interleaving for RS decoding, the advantage of the bit-level interleaving scheme becomes obvious for BCH decoding. From the overall decoding performance of concatenated codes, the improvement of BCH decoding performance makes up for the degradation of RS decoding performance and successfully improves the overall ability to resist burst errors for concatenated codes.

From all the above simulations, we can find that the bit-level interleaving schemes are suitable for burst-error channels with serious error propagation. Moreover, by considering various factors such as modulation together, we can obtain the most suitable w to get the best decoding performance.

However, when on channels with few continuous errors, like AWGN channels, the overdispersed interleaving structure is not conducive to the decoding of concatenated codes. Although the extra coding gain of the $w = 1$ symbol scheme on burst-error channels is smaller than the bit-level interleaving schemes, it can maintain performance with little loss on AWGN channels. Therefore, when the p of burst-error channels is very small and the requirement for extra coding gain is not so high, we think setting w in symbol will be a

better choice.

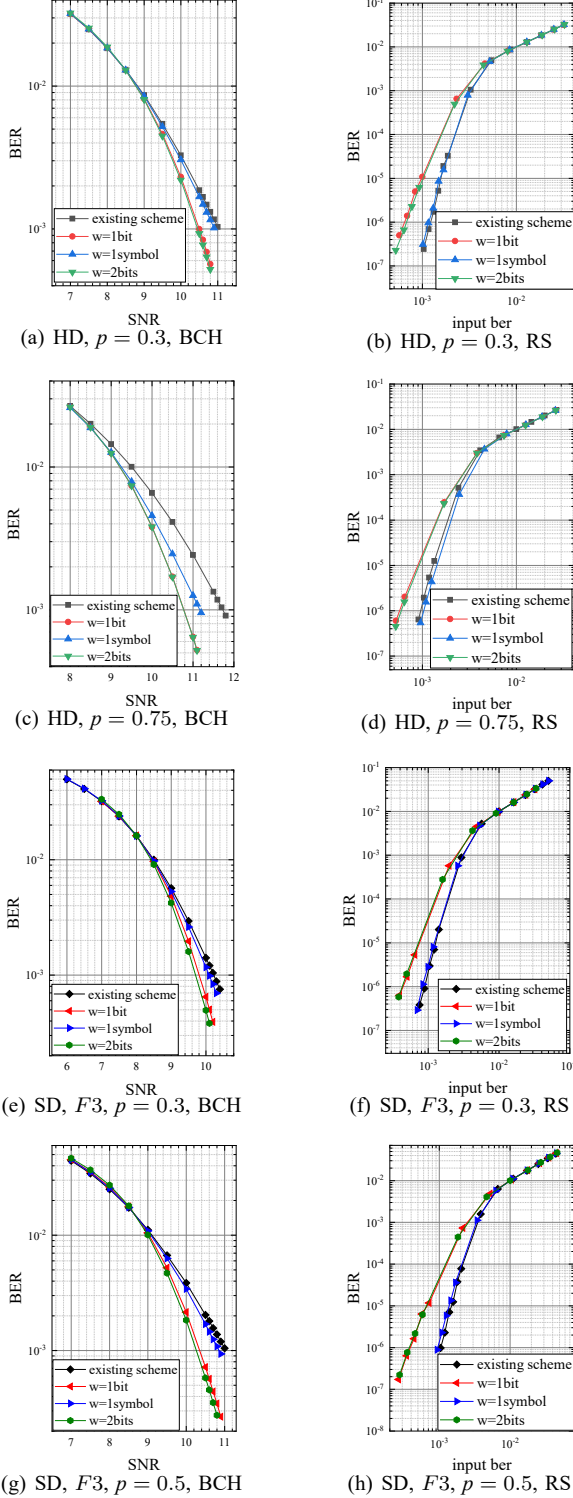


Fig. 8. BCH and RS decoding performance of four interleaving schemes on burst-error channels a) HD, $p = 0.3$, BCH; b) HD, $p = 0.3$, RS; c) HD, $p = 0.75$, BCH; d) HD, $p = 0.75$, RS; e) SD, F_3 , $p = 0.3$, BCH; f) SD, F_3 , $p = 0.3$, RS; g) SD, F_3 , $p = 0.5$, BCH; h) SD, F_3 , $p = 0.5$, RS.

Apart from the error-correction performance, we also analyze the effects of the proposed interleaving scheme on complexity and latency in brief. The matrix interleaving scheme

writes by row and reads by column. Therefore, if a BCH code will not be decoded until all the codeword bits are received, there will exist a large quantity of waiting time when realizing the proposed interleaving scheme. However, if partial-parallel decoding architecture can be used for each BCH code, the overall complexity and latency will be comparable to that of the existing interleaving scheme.

V. CONCLUSION

In this paper, we propose a novel interleaving scheme applied to concatenated codes which set KP4-FEC as outer code and BCH as inner code to improve their ability of resisting burst errors. In the proposed scheme, the continuous errors are dispersed to each BCH decoder as much as possible. Meanwhile, the errors in each symbol of RS code are still centralized by introducing a matrix interleaving. These processes greatly improve the error correction ability of concatenated codes on burst-error channels. Simulation results demonstrate that, compared with the original interleaving scheme, the new proposed interleaving scheme can achieve much better decoding performance on burst-error channels.

VI. ACKNOWLEDGMENT

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